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Quality of Electronic and Software Intellectual Property Used in System and System on Chip (SoC) Designs

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Contents

QUALITY OF ELECTRONIC AND SOFTWARE INTELLECTUAL PROPERTY USED IN SYSTEM AND SYSTEM ON CHIP (SOC) DESIGNS

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IEEE Standard for Quality of Electronic and Software Intellectual Property Used in System and System on Chip (SoC) Designs

Sponsor

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This standard contains material originally published by the VSI Alliance and currently available in the public domain (http://vsi.org/). Acknowledgment is made to the VSI Alliance, who developed the VSIA-QIP v4.0 spreadsheet and macros, and the QIP Metric Users Guide Version 4.0 document from which some material in this standard was derived.

Abstract: A standard XML format for representing electronic design intellectual property (IP) quality information, based on an information model for IP quality measurement, is defined. It includes a schema and the terms that are relevant for measuring IP quality, including the software that executes on the system. The schema and information model can be focused to represent particular categories of interest to IP users. In the context of this document, the term *IP* shall be used to mean *electronic design intellectual property.* Electronic design intellectual property is a term used in the electronic design community to refer to a reusable collection of design specifications that represent the behavior, properties, and/or representation of the design in various media.
Keywords: AMS, analog and mixed signal, design environment, EDA, electronic design automation, electronic system level, ESL, IEEE 1734, implementation constraints, MEMS, microelectromechanical systems, QIP, Quality IP metrics, register transfer logic, RTL, SCRs, semantic consistency rules, use models, verification IP, VIP, XML design meta data, XML schema

IEEE Introduction

This introduction is not part of IEEE Std 1734-2011, IEEE Standard for Quality of Electronic and Software Intellectual Property Used in System and System on Chip (SoC) Designs.

The purpose of this standard is to provide a unified view of quality measures for *electronic design intellectual property* (IP) to facilitate the use and integration of IP used in electronic system design. These quality measures can be evaluated in the context of the end application to help determine suitability and plan mitigation measures for potential integration gaps. This can enable the continuous improvement of IP used for system design and verification by providing a mechanism for qualitative comparison between such IP. The standard IP quality measures and characteristic exchange format defined can be incorporated into a variety of electronic design automation (EDA) tools. The goal of this specification is to specify a quality standard metric that will account for the variances in designing, verifying and testing the IP, which will result in fair quality assessment, reducing the risk of schedule slip or mask spins due to faulty IP.

The working group consisted of electronic system, IP provider, semiconductor, and EDA companies, and used the VSI Alliance Quality IP (QIP) metric as a baseline for the metrics. The data specified by the standard is extensible in locations specified in the schema. This structure can be used as the basis of both manual and automatic methodologies.

This standardization project provides electronic design and SoC engineers with a well-defined standard that meets their requirements in evaluating and validating IP and enables a step function increase in their productivity. This project also provides the EDA industry with a standard to which they can adhere and that they can support in order to deliver their solutions in this area.

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Quality of Electronic and Software Intellectual Property Used in System and System on Chip (SoC) Designs

1. Overview

1.1 Scope

This specification defines a standard XML format for representing electronic design intellectual property (IP) quality information, based on an information model for IP quality measurement. It includes a schema and the terms that are relevant for measuring IP quality, including the software that executes on the system. The schema and information model can be focused to represent particular categories of interest to IP users. In the context of this document, the term *IP* shall be used to mean *electronic design intellectual property*. Electronic design intellectual property is a term used in the electronic design community to refer to a reusable collection of design specifications that represent the behavior, properties, and/or representation of the design in various media.

1.2 Purpose

The purpose of this standard is to provide a unified view of quality measures for IP to facilitate the use and integration of this IP used in electronic system design. This will enable the continuous improvement of IP used for system design and verification by providing a mechanism for qualitative comparison between such

IP. The standard IP quality measures and characteristic exchange format defined can be incorporated into a variety of electronic design automation (EDA) tools.

1.3 Design environment

The IP quality specification is a mechanism to express and exchange information about design IP, its development, data management, documentation, verification and validation processes, as well as evaluating the quality and stability of the owning or development organization. While the XML description formats are the core of this standard, describing the quality specification in the context of its basic use model, the design environment (DE), more readily depicts the extent and limitations of the semantic intent of the data. The DE coordinates a set of tools and IP, or expressions of that IP (e.g., models), through the evaluation and manipulation of metadata descriptions of the IP such that the IP can be efficiently integrated into and SoC and reused.

1.3.1 Design intellectual property

Quality IP (QIP) is structured around the concept of IP reuse. *Electronic design intellectual property,* or IP, is a term used in the electronic design community to refer to a reusable collection of design specifications that represent the behavior, properties, and/or representation of the design in various media. The name IP is partially derived from the common practice of considering a collection of this type to be the intellectual property of one party. Both hardware and software collections are encompassed by this term.

Examples of these collections may include the following:

a) Design objects—This can include the following:
   1) Fixed HDL descriptions: Verilog®, VHDL[1]
   2) Verification IP descriptions: Verilog (see IEEE Std 1364™ [B2], IEC/IEEE 61691-1-1 [B1])[2]
   3) Hardened IP descriptions: GDSII, LEF, LIB, LVS, Characterization Reports
   4) Software descriptions: C, C++, etc.
   5) HDL-specified verification IP (e.g., basic stimulus generators and checkers)

b) IP views—This is a list of different views (levels of description and/or languages) to describe the IP object. These views include the following:
   1) Design view: RTL Verilog or VHDL, flat or hierarchical components
   2) Simulation view: model views, targets, simulation directives, etc.
   3) Documentation view: standard, user guide, etc.
   4) Supporting scripts: synthesis, makefile, manufacturing test, etc.

1.4 QIP-compliant enabled implementations

Complying with the rules outlined in this subclause allows the provider of tools or IP to class their products as *QIP compliant.* Conversely, any violation of these rules removes that naming right. This subclause first

[1] Verilog is a registered trademark of Cadence Design Systems, Inc. in the United States and/or other jurisdictions. This information is given for the convenience of users of this standard and does not constitute an endorsement by the IEEE of these products. Equivalent products may be used if they can be shown to lead to the same results.
[2] The numbers in brackets correspond to that of the bibliography in Annex A

introduces the set of metrics for measuring the valid use of the specifications. It then specifies when those validity checks are performed by the various classes of products and providers: DEs, point tools, and IPs.

a) Parse validity
   1) Parsing correctness: Ability to read all QIP descriptions.
   2) Parsing completeness: Cannot require information that could be expressed in a QIP format to be specified in a non-QIP format. Processing of all information present in a QIP document is not required.

b) Description validity
   1) Schema correctness: Metrics are described using XML files that conform to the QIP schema.
   2) Usage completeness: Extensions to the QIP schema shall only be used to express information that is not currently described in QIP. This information shall be forwarded to the IEEE 1734 committee for potential inclusion in a later release.

c) Semantic validity
   1) Semantic correctness: Adheres to the semantic interpretations of QIP data described in this standard.
   2) Semantic completeness: Obeys all the semantic consistency rules described in Annex B.

These validity rules can be combined with the product class specific rules to cover the full QIP-enabled space. The following subclauses describe the rules a provider has to check to claim a tool or DE is QIP compliant.

A QIP-compliant DE or point tool may read descriptions based on multiple versions of the QIP schema. If the DE or point tool does provide this capability, the effect shall be as if all of the descriptions had been translated by an XSL Transform (XSLT), which converts descriptions from one version to the next.

1.4.1 Design environments

A QIP-enabled DE:

a) Shall follow the parse validity requirements shown in 1.4.

b) Shall do so without losing any preexisting information when modifying any existing QIP descriptions. In particular, it shall preserve any vendor extension data included in the existing QIP description.

1.5 Conventions used

The conventions used throughout the document are included here.

QIP schema is case-sensitive.

1.5.1 Visual cues (meta-syntax)

Bold shows required keywords and/or special characters, e.g., addressSpace. For the initial definitional use (per element), keywords are shown in **boldface-red** text, e.g., **bitsInLau** (see also 1.6).

Bold italics shows group names or data types, e.g., ***nameGroup*** or ***boolean***.

`Courier` shows examples, external command names, directories and files, etc., e.g., address `0x0` is on `D[31:0]`.

1.5.2 Notational conventions

The keywords *required, shall, shall not, should, should not, recommended, may,* and *optional* in this document are to be interpreted as described in the IETF Best Current Practices document 14, RFC 2119 [B4].

1.5.3 Syntax examples

Any syntax examples shown in this standard are for information only and are only intended to illustrate the use of such syntax.

1.5.4 Graphics used to document the schema

The W3C® Web site specifies the XML schema language used to define the QIP XML schemas.[3, 4, 5] Normative details for compliance to the QIP standard are contained in the schema files. Within this document, pictorial representations of the information in the schema files illustrate the structure of the schema and define any constraints of the standard. With the exception of scope and visibility issues, the information in the figures and the schema files is intended to be identical. Where the figures and schema are in conflict, the XML schema file shall take precedence.

1.5.4.1 Elements and attributes

The element is the fundamental building block on which this standard is based. An element may be either a leaf element, which is a container for information, or a branch element, which may contain further branch elements or leaf elements.

A leaf or branch element may also contain attributes. Attributes are containers for information within the containing element.

1.5.4.2 Types

A type is a designation of the format for the contents of an element or attribute. There are two different styles of types that can be defined. A type may be assigned to a leaf element or an attribute. This type is called a simpleType and defines the format of data that may be stored in this container. A type may also be assigned to a branch element. This type is called a complexType and defines further elements and attributes contained in the branch element.

[3] The XML schema specification is available at http://www.w3.org/TR/2004/REC-xmlschema-1-20041028.
[4] W3C is a registered trademark of the World Wide Web Consortium (registered in numerous countries). Marks of W3C are registered and held by its host institutions: Massachusetts Institute of Technology (MIT), European Research Consortium for Information and Mathematics (ERCIM), and Keio University, Japan. This information is given for the convenience of users of this standard and does not constitute an endorsement by the IEEE of these products. Equivalent products may be used if they can be shown to lead to the same results.
[5] Information on references can be found in Clause 2.

1.5.4.3 Diagrams

The diagrams used throughout this standard graphically detail the organization the elements and attributes.

1.5.4.3.1 Elements and sequences

Figure 1 shows the sequence-compositor. At the left is a branch element, element1. **element1** is connected to a sequence-compositor. The sequence-compositor defines the order the subelements appear in the branch element. **subElement1** shall appear first inside of **element1**. This is followed by **subElement2** and **subElement3** before closing **element1**.

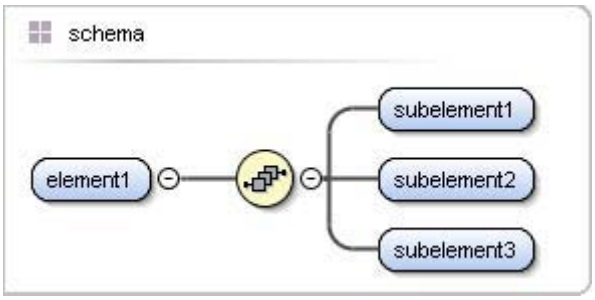

Figure 1—Sequence compositor

1.5.4.3.2 Elements and choices

Figure 2 shows the variations of the choice-compositor. **root** is connected to a choice-compositor. The choice-compositor specifies that one of the elements on the right side shall be chosen. **root** may contain one of the following: **element1**, **element2**, or **element3**. Each subelement is also connected to a choice-compositor.

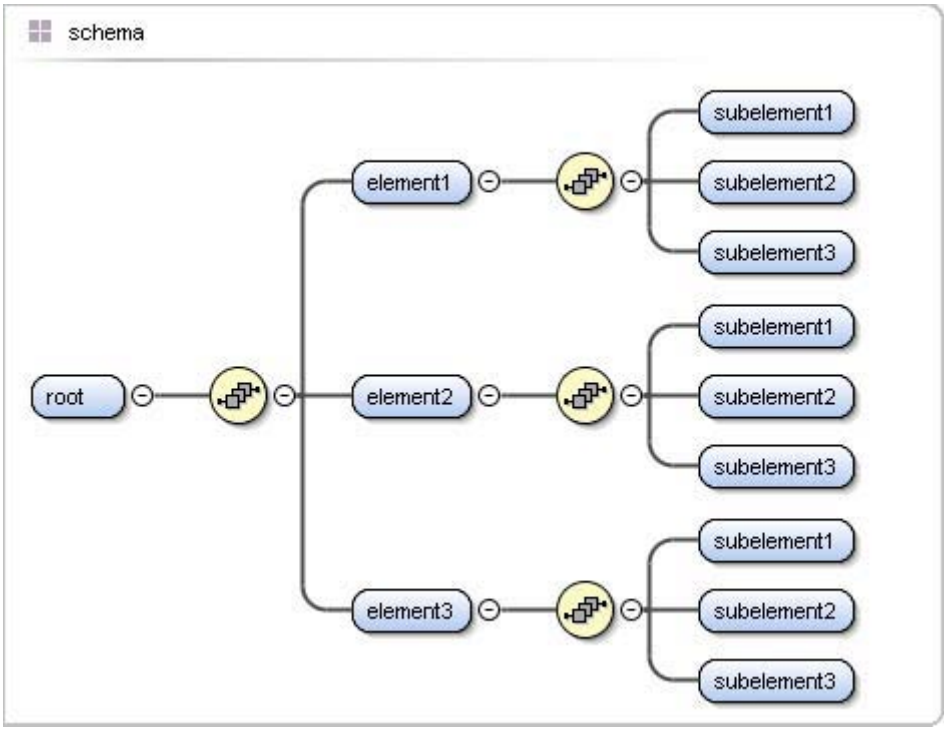

Figure 2—Choice compositor variations

1.6 Use of color in this standard

This standard uses a minimal amount of color to enhance readability. The coloring is not essential and does not affect the accuracy of this standard when viewed in pure black and white. The places where color is used are the following:

- Cross references that are hyperlinked to other portions of this standard are shown in underlined-blue text (hyperlinking works when this standard is viewed interactively as a PDF file).
- Syntactic keywords and tokens in the formal language definitions are shown in **boldface-red** text.

1.7 Contents of this standard

The organization of the remainder of this standard is as follows:

- Clause 2 provides references to other applicable standards that are assumed or required for this standard.
- Clause 3 defines terms, acronyms, and abbreviations used throughout the different specifications contained in this standard.
- Clause 4 defines the use model.
- Clause 5 describes the schema structure.
- Clause 6 describes the compatability with and differences from the VSIA QIP.

2. Normative references

The following referenced documents are indispensable for the application of this document (i.e., they must be understood and used, so each referenced document is cited in text and its relationship to this document is explained). For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments or corrigenda) applies.

W3C, XML Schema, 12 September 2005.[6]

W3C, XML Schema, Part 1: Structures, Second Edition, W3C Recommendation, 28 October 2004.[7]

[6] This specification is available at: http://www.w3.org/2001/XMLSchema; http://www.w3.org/2001/XMLSchema-instance.
[7] This specification is available at: http://www.w3.org/TR/2004/REC-xmlschema-1-20041028.